REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 6-11 are pending in the present application, Claims 6 and 9 having been amended, and Claim 12 having been canceled without prejudice or disclaimer. Support for the amendment to Claim 1 is found, for example, in Claim 12. Support for the amendment to Claim 9 is found, for example, in Fig. 3 and the corresponding description in the specification. Applicants respectfully submit that no new matter is added.

In the outstanding Office Action, Claims 9 and 12 were rejected under 35 U.S.C. § 112, second paragraph; and Claims 6-12 were rejected under 35 U.S.C. § 102(b) as anticipated by Noriyuki (JP 2003-068862).

Applicants note an Information Disclosure Statement (IDS) was filed on October 11, 2006, which at this time has been only partially indicated as considered. Specifically, on the PTO-1449 form attached to the outstanding Office Action, references AA and AB are not initialized as considered. Thus, Applicants respectfully request the Examiner to initialize as considered all the references listed on the PTO-1449 form filed with the IDS.

Regarding the rejection of Claims 9 and 12 under 35 U.S.C. § 112, second paragraph, Claim 12 has been canceled, and Claim 9 has been amended to more clearly describe and distinctly claim the subject matter regarded by Applicants as the invention. No new matter has been added. Accordingly, it is respectfully requested this rejection be withdrawn.

As an initial matter, it is noted that MPEP §706.02 II is relevant to rejections based on English Abstracts and/or the underlying foreign language document. This MPEP section makes it clear that if the Examiner is relying on both the English Abstract and the underlying Japanese document (JP 2003-068862), a translation of this document is to be obtained and supplied prior to implementing a final Action. As the present Action includes no translation

of the underlying document, the outstanding Office Action must be relying on the English Abstract alone. However, MPEP §707.02 II makes it clear that such reliance is "inappropriate where both the abstract and the underlying document are prior art."

Accordingly, it is respectfully submitted that the present Action that must be relying only on the Noriyuki English Abstract is inappropriate and should be withdrawn. Furthermore, to the extent that any subsequent Action relies on Noriyuki), a copy of the full translation should be supplied as required under MPEP §706.02 II.

As a courtesy, a machine translation of Noriyuki is filed herewith.

With respect to the rejection of Claim 6 as anticipated by Noriyuki, Applicants respectfully submit that the amendment to Claim 6 overcomes this ground of rejection. Amended Claim 6 recites, *inter alia*, "the plural components of the shield include a first and second component each having a perimeter that is partially opened, the first component and the second component are in different vertical planes, and the first and second components are arranged such that the openings in the perimeters of the first and second components are not superposed in a stacked state of the plural components." Noriyuki does not disclose or suggest these elements of amended Claim 6.

Fig. 1 of Noriyuki discloses two touch-down metal sides 11 surrounding wiring 2. The two sides 11 are on the same plane as the wiring. Thus, the two sides 11 shown in Fig. 1 of Noriyuki do not disclose or suggest the claimed "the plural components of the shield include a first and second component each having a perimeter that is partially opened, the first component and the second component are in different vertical planes, and the first and second components are arranged such that the openings in the perimeters of the first and second components are not superposed in a stacked state of the plural components."

Fig. 2 of Noriyuki is a cross-section of the structure shown in Fig. 1 of Noriyuki. This cross-section does not show that components included in the shield of Noriyuki (e.g.,

components shown within layers 8) have a perimeters that are partially opened, and that the openings in such partially opened perimeters are not superposed in a stacked state.

In view of the above-noted distinctions, Applicants respectfully submit that Claim 6 (and Claims 7-9 dependent thereon) patentably distinguish over Noriyuki.

Moreover, Applicants respectfully submit that Claims 7 and 8 further patentably distinguishes over Noriyuki.

Claim 7 recites "an interconnection width of the shield is equal to or more than a size of a spacing of the spiral pattern of the inductor, and is equal to or less than a radius of the spiral pattern of the inductor." The outstanding Office Action basis the rejection of Claim 7 on what is shown in Fig. 1 of Noriyuki. The outstanding Office Action improperly presumes that the width of metal side 1, the spacing of the spiral patter, and the radius of the spiral pattern are drawn to a particular scale in Fig. 1 of Noriyuki. No such disclosure appears in the English Abstract of Noriyuki or the enclosed machine translation.

Claim 8 recites "a distance between the shield and an outer border of the interconnection of the inductor is equal to a spacing of the spiral pattern of the inductor." The outstanding Office Action basis the rejection of Claim 8 on what is shown in Fig. 2 of Noriyuki. The outstanding Office Action improperly presumes that the distance between metal piece 11 and the wiring 2 is drawn to a particular scale in Fig. 2 of Noriyuki. No such disclosure appears in English Abstract of Noriyuki or the enclosed machine translation.

The PTO cannot simply assume that patent drawings are to scale. *See* In re Wilson, 136 USPQ 188, 192, (CCPA 1963) that specifically points our that because "[p]atent drawings are not working drawings," arguments predicated on portions of drawings "obviously never intended to show the dimensions of anything," like the arguments in the final rejection, are without merit. Further note In re Wright, 193 USPQ 332, 335 (CCPA 1977) ("Absent any written description in the specification of quantitative values, arguments

based on measurement of a drawing are of little value. In re Chitayat, 56 CCPA 1343, 408 F.2d 475, 161 USPQ 224(1969)").

With respect to the rejection of Claim 10 as anticipated by Noriyuki, Applicants respectfully traverse the rejection. Claim 10 recites, *inter alia*, "a shield that is provided with a second conductor interconnection in a ring having a continuous configuration provided along an inner periphery of the spiral pattern of the inductor...." Noriyuki does not disclose or suggest that a second conductor interconnection of a shield is provided along an inner periphery of the spiral pattern.

On the contrary, metal sides 11, which the outstanding Office Action equates to the claimed shield, are positioned to surround spiral wire 2. Noriyuki does not disclose or suggest any structure on the inner periphery of spiral wire 2.

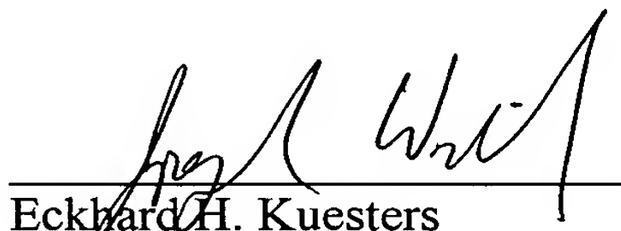
In view of the above-noted distinction, Applicant respectfully submits that Claim 10 (and Claim 11 dependent thereon) patentably distinguishes over Noriyuki.

Moreover, Applicants respectfully submit that Claim 11 further patentably distinguishes over Noriyuki. As noted above for Claims 7 and 8, the outstanding Office Action again errs by making the improper presumption that the figures of Noriyuki are drawn to scale when rejecting Claim 11.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Joseph Wrkich
Registration No. 53,796

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the structure of the spiral inductance constituted using the manufacture process of a semiconductor device.

[0002]

[Description of the Prior Art] Generally a spiral inductor is used for the RF circuit of an integrated circuit as an inductor. A spiral inductor is an inductor of the multilayer interconnection which formed wiring in the shape of a spiral (spiral) on the flat surface, and shows the example to drawing 6 and drawing 7 . Drawing 6 is the plan of the spiral inductor formed in the semiconductor device. Drawing 7 is the A-A' sectional view of a spiral inductor shown in drawing 6 .

[0003] As shown in drawing 6 , the spiral inductor 121 is constituted by the through hole 115 for connecting the wiring 102 of the shape of a spiral formed on the maximum upper insulating layer 116 of a semiconductor device 101, the wiring 103 of the shape of a straight line formed on insulating layer (here layer insulation layer of the maximum upper layer to a two-layer eye) 117 with the another maximum upper insulating layer 116, wiring 102, and wiring 103. Moreover, one terminal 114 of the spiral inductor 121 is formed in the edge of the spiral-like wiring 102, and it connects with the terminal of an external circuit (not shown) etc. Furthermore, the other-end child 113 of the spiral inductor 121 is formed in the edge of the straight-line-like wiring 103, and it connects with the terminal of an external circuit (not shown) etc.

[0004] Moreover, the cross-section structure of the conventional spiral inductor forms wiring 102 on the maximum upper insulating layer 116 through two or more layer insulation layers on SiO2 film formed on the semi-conductor substrate 106, as shown in drawing 7 . The spiral inductor 121 is formed by forming the wiring 102 on the maximum upper insulating layer 116 in the shape of a spiral.

[0005] In addition, by drawing 7 , two or more insulating layers 108 show the example which is 10 lamination. Two or more insulating layers 108 are formed for component formation of the analog circuit section outside drawing, and the digital circuit section, or a multilayer interconnection.

[0006] The above spiral inductors of a configuration are used as the impedance matching circuit for transmitting power efficiently in a RF circuit, and a resonance circuit for maintaining vibration of an oscillator regularly.

[0007] Conventionally, since electron mobility was high, compound semiconductors, such as GaAs which can form a transistor with a good high frequency property, were used for the process of a high frequency integrated circuit in many cases. In the spiral

inductor which such a compound semiconductor is a half-insulator, and was formed on the semi-insulating substrate, especially the parasitic capacitance between substrates did not become a problem. Moreover, the semiconductor device using a compound semiconductor is in the situation that even what formed analog circuits, such as an amplifying circuit and a mixer, to current is developed, and has not resulted to the thing which made digital circuits, such as the logic section, load together in the same semiconductor device as the above-mentioned analog circuit. Therefore, the diving noise from the digital circuit generated when an analog circuit and a digital circuit are loaded together in the same semiconductor device to an analog circuit has not been a problem.
[0008] However, detailed-ization in a silicon process progresses with an advance of a technique in recent years, a transistor with a good high frequency property can be formed now on a silicon substrate, and formation on a silicon substrate has been attained in the high frequency integrated circuit. Since using a silicon process and making a logical circuit load together on the silicon substrate in which the spiral inductor was formed can carry out easily, it will be in the condition that the problem of the noise through the substrate of spiral in DAKUTAHE formed on the semi-conductor substrate is not avoided from a digital circuit.
[0009] Moreover, a silicon substrate is a semi-conductor substrate, and since the insulating layer is prepared between the spiral inductor and the substrate, the parasitic capacitance between a spiral inductor and a substrate also poses a problem. That is, especially in a spiral inductor, since the wiring 102 of the shape of a spiral formed in the upper wiring layer is comparatively large in area, parasitic capacitance will be formed between wiring 102 and the semi-conductor substrate 106 through the layer insulation layer 108.
[0010] Furthermore, although the wiring 102 of the shape of a spiral formed in the maximum upper insulating layer 116 is not illustrated, if the output signal in an amplifying circuit etc. jumps in through the layer insulation layer 108 or a semi-conductor substrate and spreads as a noise from it being comparatively large in area as mentioned above even in the signal of the digital circuit section, and an analog circuit, as for the RF circuit using this spiral inductor, it will become easy to receive a bad influence.
[0011] So, the technique about the spiral inductor which inserted the polish recon layer in the direct lower layer section of an inductor is indicated by the JP,2000-188373,A official report. This spiral inductor can reduce the phase noise of an oscillator circuit, when the parasitism resistance and parasitic capacitance which are attached to an inductor by having made the polish recon layer into a substrate substrate and same electric potential can be made small and an inductor is made into a part of resonance circuit of a dispatch circuit.
[0012]
[Problem(s) to be Solved by the Invention] However, by the above-mentioned approach, the parasitic capacitance between wiring-polish recons becomes large, and the property of a spiral inductor deteriorates remarkably. Moreover, the propagation of a noise from the perimeter of a spiral inductor can be considered through a layer insulation layer.
[0013] Then, it is that create this invention in order to solve the above-mentioned problem, and the purpose reduces the amount of propagation of the noise through the substrate-insulating layer of spiral in DAKUTAHE formed on the semi-conductor substrate in the silicon process, and the noise from a logical circuit does not have a bad

influence on a RF circuit. Moreover, it is stopping small the parasitic capacitance formed in this invention between the parts and spiral inductors which reduce a diving noise, and not causing property degradation of an inductor.
[0014]
[Means for Solving the Problem] This invention is equipped with the following configurations as above-mentioned The means for solving a technical problem.
[0015] (1) It is characterized by equipping with the shielding section the perimeter of spiral-like wiring formed of the silicon process on the predetermined layer of the semiconductor device equipped with two or more insulating layers.
[0016] In this configuration, the spiral inductor equips with the shielding section the perimeter of spiral-like wiring formed of the silicon process on the predetermined layer of the semiconductor device equipped with two or more insulating layers. Therefore, when digital circuits, such as a logical circuit, are formed on the same substrate of spiral in DAKUTAHE, the noise propagation from a digital circuit decreases remarkably, and becomes possible [controlling the bad influence to a RF circuit].
[0017] (2) said shielding section is characterized by to have come out with the connection which connects electrically the touch-down conductivity side formed in the perimeter of said spiral-like wiring, the conductive field formed on the layer in which said spiral-like wiring was formed, one layer, or the layer left two or more layers, and this touch-down conductivity side and this conductive field, and to consist of on the same layer as said spiral-like wiring.
[0018] a spiral inductor is equipped with the connection which connects electrically the touch-down conductivity side formed in the perimeter of spiral-like wiring on the same layer as spiral-like wiring, the conductive field formed on the layer in which spiral-like wiring was formed, one layer, or the layer left two or more layers, and a touch-down conductivity side and a conductive field, and the shielding section which were come out of and constituted in this configuration. Therefore, it becomes possible to reconcile a shielding effect and reduction of the parasitic capacitance of spiral in DAKUTAHE by this shielding section.
[0019] (3) Said conductive field is characterized by being formed with a substrate wiring material.
[0020] The shielding section of a spiral inductor is equipped with the conductive field formed with the substrate wiring material in this configuration. Therefore, manufacture is easy and does not cause a cost rise.
[0021] (4) Said conductive field is characterized by being formed by polish recon.
[0022] The shielding section of a spiral inductor is equipped with the conductive field formed by polish recon in this configuration. Therefore, manufacture is easy and can control the rise of cost.
[0023] (5) two or more through hole **** by which said connection was arranged in the perimeter of said spiral-like wiring -- it is characterized by things.
[0024] The connection of a spiral inductor is constituted in this configuration by two or more through holes arranged in the perimeter of spiral-like wiring. Therefore, it becomes possible by easily realizable technique to connect a touch-down conductivity side and a conductive side.
[0025] (6) Said connection is characterized by being the groove crevice arranged in the perimeter of said spiral inductor.

[0026] The connection of a spiral inductor is constituted in this configuration by the groove crevice arranged in the perimeter of a spiral inductor. Therefore, it becomes possible to heighten a shielding effect further.
[0027] It is characterized by equipping either (7), (1) or (6) with the spiral inductor of a publication.
[0028] In this configuration, high frequency semiconductor equipment equips either (1) thru/or (6) with the spiral inductor of a publication. Therefore, since an inductor strong against a noise can be formed, it is effective in lightweight-izing of a cellular phone etc., and a miniaturization to be able to realize an analog circuit and the high frequency semiconductor equipment of digital circuit mixed loading, and for mixed loading of a digital processing circuit to be attained by this in the amplifying circuit of the input section of the cellular phone using a GIGAHERUTSU band etc.
[0029]
[Embodiment of the Invention] Drawing 1 is the plan of the spiral inductor concerning the 1st operation gestalt of this invention. Moreover, drawing 2 is the A-A' sectional view of a spiral inductor shown in drawing 1 . The spiral inductor 21 shown in drawing 2 is equipped with the insulating layer 8 of 10 lamination.
[0030] Here, only the spiral inductor concerning the operation gestalt of this invention is shown in drawing 1 and drawing 2 , and other analog circuits and digital circuit sections which constitute a semiconductor device are omitted in order to make it constitute from an existing technique.
[0031] The configuration of the ten-layer layer insulation layer 8 (here SiO2) formed on the semi-conductor substrate 6 (here Si) is explained to an example. In addition, the protective layer for protecting the metal wiring 2 grade on the maximum upper insulating layer 16 is omitting illustration. Moreover, the ten-layer layer insulation layer 8 is formed for component formation of the analog circuit section which is not illustrated and the digital circuit section, or a multilayer interconnection.
[0032] As shown in drawing 1 , the spiral inductor 21 The metal wiring 2 of the shape of a spiral formed on the maximum upper insulating layer 16 of two or more insulating layers 8 formed on the semi-conductor substrate 6, An insulating layer which is different in the maximum upper insulating layer 16 for the outgoing line from the core of the spiral-like wiring 2 (here) it comes out with the through hole 15 for performing wiring 3 and electrical installation, and consists of the maximum upper layers at the core of the shape of a spiral of the metal wiring 3 formed on the layer insulation layer of a two-layer eye, and wiring 2. In addition, wiring 2 and wiring 3 are formed with substrate wiring materials, such as for example, aluminum wiring and copper wiring.
[0033] Moreover, the terminal 14 for pulling out wiring 2 and connecting it with other circuits which are not illustrated is formed in the edge of wiring 2, and the terminal 13 for connecting wiring 3 with other circuits which are not pulled out and illustrated is formed in the edge of wiring 3.
[0034] Next, the characteristic configuration of this invention is explained. In this invention, as shown in drawing 2 , the metal side 5 which is a conductive side of size larger than the periphery section of the spiral inductor 21 as a wiring layer on the lowest layer insulating layer 7 formed on the semi-conductor substrate 6 is formed. On the other hand, the touch-down metal side 1 which is a touch-down conductivity side is formed in the periphery of the spiral inductor 21 as a wiring layer on the maximum upper insulating

layer 16 (the same field as wiring 2). In addition, the metal side 5 and the touch-down metal side 11 are formed with substrate wiring materials, such as for example, aluminum wiring and copper wiring, and the touch-down metal side 11 is grounded with wiring outside drawing.

[0035] Furthermore, it connects in two or more through holes 4 the metal side 5 and whose touch-down metal sides 11 are connections which penetrate the layer insulation layer 8. Here, two or more through holes 4 are perpendicularly formed to the field in which the spiral inductor 21 was formed.

[0036] thus, since it constitutes, the spiral inductor 21 formed on the semi-conductor substrate which constitutes a semiconductor device through an insulating layer according to a silicon process will be shielded by the touch-down metal side 11 on the maximum upper insulating layer 16, the metal side 5 on the lowest layer insulating layer 7, two or more through holes 4 currently arranged around the spiral inductor 21, and the shielding section come out of and constituted.

[0037] Thereby, although not illustrated, the effect through the semi-conductor substrate and two or more insulating layers from the analog circuit currently formed in the same semi-conductor substrate or a digital circuit of a diving noise can be decreased remarkably.

[0038] Moreover, the field in which the spiral inductor 21 is formed is forming in one layer or the layer left two or more layers, and since the metal side 5 keeps its distance and can form both sides, it can prevent degradation of the inductor property can carry out things and according to parasitic capacitance to which parasitic capacitance is made small.

[0039] Furthermore, what is necessary is just to set up two or more through holes 4 which connect the metal side 5 and the touch-down metal side 11 by adjusting the number to form, or adjusting and arranging spacing, so that a shielding effect may go up.

[0040] In addition, the path of a through hole 4 may be enlarged, it may replace with a through hole, a slot (crevice) may be formed in two or more insulating layers 8, and the metal side 5 and the touch-down metal side 11 may be connected. Moreover, a slot may be extended extensively and the circumference of the spiral inductor 21 except the terminal area of a spiral inductor may be enclosed. However, connection by the through hole is technique easily realizable among the general techniques to which between insulating layers is connected.

[0041] Moreover, among two or more insulating layers 8, whether a spiral inductor, the metal side 5, and the touch-down metal side 11 are formed takes a shielding effect and parasitic capacitance into consideration in which layer, and it should just set it as. Therefore, as shown in drawing 2 , the spiral inductor 21, the metal side 5, and the touch-down metal side 11 may be formed in addition to maximum upper insulating-layer 16 and lowest layer insulating-layer 7.

[0042] Furthermore, the spiral inductor 21 can be formed on the layer insulation layer of the arbitration in two or more insulating layers 8, the touch-down metal side 11 of the maximum upper insulating layer 16 can be made into the metal side of size larger than the periphery section of the spiral inductor 21, and the perimeter of the spiral inductor 21 can be enclosed in the shielding section by connecting the metal side 5 and the touch-down metal side 11 in two or more through holes 4.

[0043] Moreover, it becomes possible to reduce the noise emitted from an analog circuit or a digital circuit by extending and forming in the analog circuit and the digital circuit

section outside drawing the touch-down metal side 11 formed in the perimeter of the spiral inductor 21 at the same flat surface as the spiral inductor 21.
[0044] Next, the effectiveness which prepared the shielding section is explained using the equal circuit of a spiral inductor. Drawing 8 is the representative circuit schematic showing the noise propagation in the conventional spiral inductor shown in drawing 6 and drawing 7 . The equal circuit of the spiral inductor 21 shown in drawing 8 is the case where ten layers of insulating layers are prepared, and each dimension of a spiral inductor is track width-of-face [of 15 micrometers], and track tooth-space 5micrometer, and 4000 micrometers of track length. Moreover, an insulating layer 8 consists of SiO2, and the thickness of one layer is 1.5 micrometers. Furthermore, in the equal circuit of a spiral inductor, R2 and parasitic capacitance are expressed for the wiring resistance which is equivalent to C1 and the semi-conductor substrate 6 in the parasitic capacitance according wiring resistance to R1 and an insulating layer 8 according an inductance value to L1 as C2. In addition, it was referred to as R3=10kohm as a model in which propagation of a noise is shown. It shall generate from a noise source 40 and a noise signal shall be spread from a substrate front face to the spiral inductor 21 through the layer insulation layer 8. The estimate of the amount of propagation of a noise is given with the power through put from the noise source 10 to the I/O sections 41 and 42 of the spiral inductor 21.
[0045] Drawing 3 is the representative circuit schematic showing the noise propagation in the spiral inductor concerning the 1st operation gestalt of this invention. This equal circuit is computed from the conventional example shown in drawing 8 in consideration of the spiral cross-section structure in the 1st operation gestalt of this invention. The 1st operation gestalt and the conventional example of this invention make the circuit pattern of a spiral inductor the same thing. With the 1st operation gestalt of this invention, as shown in the sectional view of drawing 2 , the lowest layer metal side 5 is connected to the metal ground plane 1 in the through hole 4. In this case, the inductance value L1 which is a value specified with the circuit pattern of the spiral inductor 21, the wiring resistance R1, the wiring resistance R2 equivalent to the semi-conductor substrate 6, and parasitic capacitance C2 serve as the same value in the 1st operation gestalt and the conventional example of this invention. The parasitic capacitance by the insulating layer 8 is set to C1a (capacity which is a part for nine layers of insulating layers), and C1b (capacity which is a part for one layer of insulating layers) according to the lowest layer metal side 5. The contact resistance at the time of the lowest layer metal 5 being connected to the metal touch-down wiring 1 in a through hole 4 is expressed as R4. With this operation gestalt, it calculated by 5ohm and the layer / hole as a typical value of the through hole formed in a silicon process. And the total of a through hole was made into 45 pieces, and connection through nine layers of insulator layers was assumed. Consequently, they could be R4=5 ohm/hole x9 layer / 45 pieces = 1.0 ohms.
[0046] Drawing 4 is the graph which showed the noise propagation simulation result by the spiral inductor in the 1st operation gestalt and the conventional example of this invention. The amount of noise propagation is -89dB in this invention in a 2-3GHz band. Therefore, as compared with -51dB which is the amount of noise propagation of the conventional example, the amount of 48dB noise propagation has been reduced. In addition, in a 2-3GHz band, although the property improvement at the time of using the spiral inductor of this invention was shown, a frequency band is an example and does not

limit the frequency band of this invention.
[0047] From this result, it has checked that the effect of the noise from the logical circuit by which this invention is formed on the same substrate through the semi-conductor substrate using the equal circuit decreased remarkably.
[0048] Next, the spiral inductor concerning the 2nd operation gestalt of this invention is explained. Drawing 5 is the sectional view of the spiral inductor concerning the 2nd operation gestalt of this invention. Since the configuration of the spiral inductor concerning the 2nd operation gestalt of this invention is the same as the spiral inductor 21 concerning the 2nd operation gestalt of this invention, explanation here is omitted.
[0049] In the spiral inductor 31 concerning the 2nd operation gestalt of this invention, it replaces with the metal side 5 which constitutes the shielding section of the spiral inductor 21, and the polish recon side with conductivity is used. That is, polish recon (polish recon currently used at the gate etc.) with conductivity is arranged on the semi-conductor substrate 6 (here Si). And it has connected electrically by two or more through holes 4 which penetrate the touch-down metal side 11 currently formed in the maximum upper insulating layer 16, and the layer insulation layer 8 (here SiO2) like the 1st operation gestalt of this invention.
[0050] The spiral inductor 31 formed on the semi-conductor substrate through the insulating layer by doing in this way of the silicon process will be shielded by the shielding section constituted by the touch-down metal side 11 on the maximum upper insulating layer 16, the polish recon side 9 on the semi-conductor substrate 6, and two or more through holes 4 currently arranged around the spiral inductor 31.
[0051] In this case, the layer insulation layer formed between the polish recon side 9 and the touch-down metal side 2 turns into ten layers, the layer insulation layer is increasing one layer as compared with the 1st operation gestalt of nine layers, and it is effective in lowering parasitic capacitance more.
[0052] In addition, although the operation gestalt of this invention explained the configuration which used the silicon process and prepared a spiral inductor and the shielding section on Si substrate, it is not limited to this, can apply also to the semiconductor device formed by SiGe (silicon germanium) on Si substrate, and is effective in the semiconductor device using a layer insulation layer.
[0053] It consists of connecting means which connect electrically the touch-down conductivity side formed in the field as spiral-like wiring which forms a spiral inductor where this invention is the same as mentioned above, the conductive field formed in the field which minded the layer insulation layer in the field which forms a spiral inductor, and these both sides, and reduction of the parasitic capacitance of spiral in DAKUTAHE by this shielding means is reconciled with a shielding effect.
[0054] Moreover, since it can constitute from a known technique, it does not become a cost rise factor.
[0055] It is effective in lightweight-izing of a cellular phone, and a miniaturization to be able to realize an analog circuit and the high frequency semiconductor equipment of digital circuit mixed loading by the ability of a spiral inductor strong against a noise to be formed, and for mixed loading of a digital processing circuit to be attained by this in the amplifying circuit of the input section of the cellular phone using a GIGAHERUTSU band etc.
[0056]

[Effect of the Invention] According to this invention, the following effectiveness is acquired.

[0057] (1) When a spiral inductor forms digital circuits, such as a logical circuit, on the same substrate of spiral in DAKUTAHE by equipping with the shielding section the perimeter of spiral-like wiring formed of the silicon process on the predetermined layer of the semiconductor device equipped with two or more insulating layers, the noise propagation from a digital circuit decreases remarkably, and it can control the bad influence to a RF circuit.

[0058] (2) The touch-down conductivity side where the spiral inductor was formed in the perimeter of spiral-like wiring on the same layer as spiral-like wiring, since it has the connection which connects electrically the conductive field formed on the layer in which spiral-like wiring was formed, one layer, or the layer left two or more layers, and a touch-down conductivity side and a conductive field, and the shielding section come out of and constituted A shielding effect and reduction of the parasitic capacitance of spiral in DAKUTAHE by this shielding section can be reconciled.

[0059] (3) Since the shielding section of a spiral inductor is equipped with the conductive field formed with the substrate wiring material, it is easy, and manufacture does not cause a cost rise but is effective for cost control.

[0060] (4) Since the shielding section of a spiral inductor is equipped with the conductive field formed by polish recon, it is easy to manufacture and can control the rise of cost.

[0061] (5) Since the connection of a spiral inductor is constituted by two or more through holes arranged in the perimeter of spiral-like wiring, it is easily realizable technique and can connect a touch-down conductivity side and a conductive field.

[0062] (6) Since the connection of a spiral inductor is constituted by the groove crevice arranged in the perimeter of a spiral inductor, it can heighten a shielding effect further.

[0063] (7) a cellular phone -- since high frequency semiconductor equipment can form an inductor strong against a noise by equipping either (1) thru/or (6) with the spiral inductor of a publication, it can realize an analog circuit and the high frequency semiconductor equipment of digital circuit mixed loading, and mixed loading of a digital processing circuit of it is attained by this in the amplifying circuit of the input section of the cellular phone using a GIGAHERUTSU band -- etc. -- lightweight-izing -- it can miniaturize.

[Translation done.]